L3: Entry 3 of 11 File: USPT Mar 2, 2004

DOCUMENT-IDENTIFIER: US 6700877 B1
TITLE: Method and bus system for automatic address allocation

Abstract Text (1):
A method for automatic address assignment is disclosed, said method being based on a distance measurement, a master (M) transmitting via the bus a preamble (P) which is received by all the slaves which are to be addressed. The slaves react to the preamble (P) by transmitting a response signal sequence (A). A slave (S2) which is located upstream, in the direction of the master (M), of a slave (S3) which transmits a response signal sequence (A) registers the response signal sequence (A) of the slave (S3) and subsequently waits for a new preamble (P). The slave (Sz) which does not register any response signal sequences (A) from other slaves is the last slave (Sz), seen from the master (M), without address allocation on the bus. This slave (Sz) switches into a state in which it is ready to receive an address-assigning telegram (T) from the master (M), with which address-assigning telegram (T) it is assigned an unambiguous address. During the next cycle of the method, the slave (Sz) which has just been assigned an address no longer reacts to the preamble (P) so that another slave evaluates the constellations at the bus in such a way that it switches into a state in which it is ready to receive the address-assigning telegram. In this way, all the slaves without an address are gradually assigned an address.

Detailed Description Text (10):
During the automatic address assignment, during which the slaves S1, S2, . . . which have not yet been assigned an address are therefore in the configuration mode K, the master, which initiates the method according to the invention for automatic address assignment, seizes the bus in order to transmit a signal sequence and, if appropriate, monitor the reception of response signal sequences. The slaves S1, S2, . . . , which are not tied to a bus protocol during the operation in the configuration mode K, detect received signal sequences in accordance with their internal wiring which is suitable for executing the method according to the invention, and furthermore, if appropriate, they transmit their own signal sequences in reaction to the received signal sequences without, in doing so, having to take into account possible further data traffic on the communications medium.

Detailed Description Text (47):
However, it is equally possible for the slaves S1, S2,. . . , as further described above, to be numbered in an ascending or descending order and to be assigned in each case an address which corresponds to this numbering. Thus, for example a slave S1 at a distance of 5 m from the master M has the address "1", a slave S2 at a distance of 7 m from the master has the address "2" and a slave S3 at a distance of 12 m from the master has the address "3". In this case, the master M advantageously manages a lookup table LUT from which an allocation between the assigned addresses and the time differences t determined during the address assignment can be obtained; LUT=[(1; 5 m), (2; 7 m), (3; 12 m)]. In this case, the information item relating to position in the lookup table LUT can be obtained at the position which is defined by the respective address. Thus, it is also possible for slaves S1, S2, . . . which are added later to perform automatic addressing and to determine the information item relating to position. A newly added slave S4 at a distance of 9 m from the master M can, without renumbering the slaves S1, S2, S3 which have already been addressed, not be incorporated into a bus with an address which ascends monotonously in relation to the distance from the master; instead, the next free address "4" is assigned to the newly added slave S4, in which case, however, by reference to the propagation time difference t whose distance from the master M can be determined unambiguously, with the result that the information item relating to position is available again by means of the lookup table LUT=[(1; 5 m), (2; 7 m), (3; 12 m), (4; 9 m)].

Detailed Description Text (59):

In conclusion,, the present invention can be summarized in brief as follows: a method which is based on a distance measurement is specified for automatic address assignment, a master M transmitting over the bus a preamble P which is received by all the slaves S1, S2, . . . which are to be addressed. The slaves S1, S2, . . . react to the preamble P) by transmitting a response signal sequence A. A slave S2 which is located, in the direction of the master M, upstream of a slave S3 which transmits a response signal sequence A, registers the response signal sequence A of the slave S3 and subsequently waits for a new preamble P. The slave SZ which does not register any response signal sequences A from other slaves S1, S2, . . . is the, viewed from the master M, last slave Sz without address allocation the bus. This slave Sz switches to a state in which it is ready to receive an address-assigning telegram T from the master M, with which address-assigning telegram T it is assigned an unambiguous address. During the next cycle of the method, the slave Sz which has just been assigned an address no longer reacts to the preamble P, with the result that another slave S1, S2, . . . evaluates the constellations on the bus in such a way that it switches itself to a state in which it is ready to receive the address-assigning telegram T. In this way, all the slaves S1, S2, . . . without an address are gradually assigned one.

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L3: Entry 5 of 11 File: USPT Dec 28, 1999

US-PAT-NO: 6009479
DOCUMENT-IDENTIFIER: US 6009479 A

TITLE: System and method for assigning unique addresses to agents on a system management bus

DATE-ISSUED: December 28, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jeffries; Kenneth Layton	Leander	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell USA, L.P.	Round Rock	TX			02

APPL-NO: 08/ 866678 [PALM]
DATE FILED: May 30, 1997

PARENT-CASE:
This application is a continuation-in-part of copending patent application Ser. No. 08/389,849, filed on Feb. 17, 1995, and entitled "System And Method For Assigning Unique Addresses To Agents On A System Management Bus", by Kenneth L. Jeffries, now U.S. Pat. No. 5,636,342 and which is incorporated herein by reference in its entirety.

INT-CL: [06] G06 F 11/00, G06 F 3/00

US-CL-ISSUED: 710/8; 710/62
US-CL-CURRENT: 710/8; 710/62

FIELD-OF-SEARCH: 395/828, 395/829, 395/830, 395/831, 395/832, 395/833, 395/874, 395/882, 710/8-14, 710/62

PRIOR-ART-DISCLOSED:

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Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4679192	July 1987	Vanbrabant	
☐	4701878	October 1987	Gunkel et al.	
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☐	5483518	January 1996	Whetsel	
☐	5499374	March 1996	Di Giulio et al.	
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☐	5708831	January 1998	Schon	395/829

ART-UNIT: 271

PRIMARY-EXAMINER: Sheikh; Ayaz R.

ASSISTANT-EXAMINER: Wiley; David A.

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin & Friel LLP Koestner; Ken J.

ABSTRACT:

A computer system including a bus master performs a method for automatically assigning addresses to agents on a bus. Addresses are automatically assigned so that a computer system user does not set physical or logical switches, either manually or through software programming. The system and method also automatically assign unique addresses to new devices that are inserted on the bus while the bus is operating, thereby supporting "hot pluggable" devices. Slave agents are originally configured to operate at a class address. At the beginning of the method, a master determines whether any of the slaves reside at the class address. If so, then the master determines a new unique address and issues a Get Bitwise UID command to the slaves residing at the class address. Each of the slaves receives the Get Bitwise UID and responsively transmits a hardware identification (UID) in a loop of bitwise byte transmissions. One slave successfully transmits the hardware identification (UID) while the other individual slaves detect transmission errors during transmission of the hardware identification (UID) and terminate transmission upon the error detection. The unsuccessful slaves, if previously residing at a unique address, revert to the class address. The master receives the hardware identification (UID) of the successfully transmitting slave and issues a Set Address command in combination with the hardware identification (UID) and the new unique address to all slave agents at the class address. Only the slave agent with a hardware identification (UID) matching the UID of the Set Address command processes the Set Address command to completion and is assigned the address. The master uses the Get Bitwise UID command followed by the Set Address command in a loop to locate, identify and assign addresses to agents responding to a predetermined class address.

31 Claims, 6 Drawing figures

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L3: Entry 5 of 11 File: USPT Dec 28, 1999

DOCUMENT-IDENTIFIER: US 6009479 A
TITLE: System and method for assigning unique addresses to agents on a system management bus

Brief Summary Text (13):
In an illustrative embodiment, the bus is a system management bus (SMB) operating according to an I.sup.2 C serial protocol. The system management bus (SMB) includes one or more SMB masters and a plurality of SMB slaves. The SMB master and SMB slaves perform predetermined monitoring and control operations in the computer system. The SMB master performs a method for assigning unique addresses to each of the SMB slaves automatically and without user intervention. The disclosed method and system for automatic assignment of addresses advantageously simplifies, improves efficiency, and avoids error in assigning addresses to bus agents in comparison to conventional manual and software programming techniques.

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US006700877B1

(12) **United States Patent**
Lorenz et al.

(10) **Patent No.: US 6,700,877 B1**
(45) **Date of Patent: Mar. 2, 2004**

(54) **METHOD AND BUS SYSTEM FOR AUTOMATIC ADDRESS ALLOCATION**

(75) Inventors: Joachim Lorenz, Hemhofen (DE); Karl Weber, Altdorf (DE)

(73) Assignee: Siemens Aktiengesellschaft, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/485,212

(22) PCT Filed: Jul. 23, 1998

(86) PCT No.: PCT/DE98/02076

§ 371 (c)(1),
(2), (4) Date: Feb. 4, 2000

(87) PCT Pub. No.: WO99/08164

PCT Pub. Date: Feb. 18, 1999

(30) **Foreign Application Priority Data**

Aug. 5, 1997 (DE) 197 33 906

(51) Int. Cl.[7] H04L 12/28

(52) U.S. Cl. 370/254; 370/471

(58) Field of Search 370/254, 471, 370/457; 340/825.52; 714/48

(56) **References Cited**

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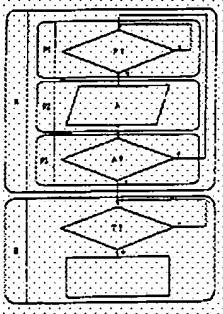
Primary Examiner—Salvatore Cangialosi
(74) *Attorney, Agent, or Firm*—Staas & Halsey LLP

(57) **ABSTRACT**

A method for automatic address assignment is disclosed, said method being based on a distance measurement, a master (M) transmitting via the bus a preamble (P) which is received by all the slaves which are to be addressed. The slaves react to the preamble (P) by transmitting a response signal sequence (A). A slave (Sj) which is located upstream, in the direction of the master (M), of a slave (Sj) which transmits a response signal sequence (A) registers the response signal sequence (A) of the slave (Sj) and subsequently waits for a new preamble (P). The slave (Sx) which does not register any response signal sequences (A) from other slaves is the last slave (Sz), seen from the master (M), without address allocation on the bus. This slave (Sz) switches into a state in which it is ready to receive an address-assigning telegram (T) from the master (M), with which address-assigning telegram (T) it is assigned an unambiguous address. During the next cycle of the method, the slave (Sz) which has just been assigned an address no longer reacts to the preamble (P) so that another slave evaluates the constellations at the bus in such a way that it switches into a state in which it is ready to receive the address-assigning telegram. In this way, all the slaves without an address are gradually assigned an address.

19 Claims, 5 Drawing Sheets



US006009479A

United States Patent [19]

Jeffries

[11] Patent Number: 6,009,479

[45] Date of Patent: Dec. 28, 1999

[54] **SYSTEM AND METHOD FOR ASSIGNING UNIQUE ADDRESSES TO AGENTS ON A SYSTEM MANAGEMENT BUS**

[75] Inventor: **Kenneth Layton Jeffries**, Leander, Tex.

[73] Assignee: **Dell USA, L.P.**, Round Rock, Tex.

[21] Appl. No.: **08/866,678**

[22] Filed: **May 30, 1997**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/389,649, Feb. 17, 1995, Pat. No. 5,630,142.

[51] Int. Cl.[6] G06F 11/00; G06F 3/00

[52] U.S. Cl. 710/8; 710/62

[58] Field of Search 395/825, 829, 395/830, 831, 832, 833, 874, 682, 710/8–14, 62

[56] **References Cited**

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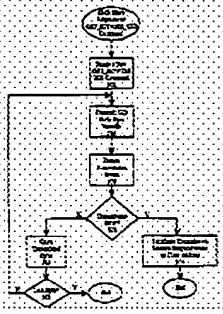
Primary Examiner—Ayaz R. Sheikh
Assistant Examiner—David A. Wiley
Attorney, Agent, or Firm—Sprinkle, Merrill, MacPherson, Franklin & Friel LLP; Ken J. Koestner

[57] **ABSTRACT**

A computer system including a bus master performs a method for automatically assigning addresses to agents on a bus. Addresses are automatically assigned so that a computer system user does not set physical or logical switches, either manually or through software programming. The system and method also automatically assign unique addresses to new devices that are inserted on the bus while the bus is operating, thereby supporting "hot-pluggable" devices. Slave agents are originally configured to operate at a class address. At the beginning of the method, a master determines whether any of the slaves reside at the class address. If so, then the master determines a new unique address and issues a Get Bitwise UID command to the slaves residing at the class address. Each of the slaves receives the Get Bitwise UID and responsively transmits a hardware identification (UID) in a loop of bitwise byte transmissions. One slave successfully transmits the hardware identification (UID) while the other individual slaves detect transmission errors during transmission of the hardware identification (UID) and terminate transmission upon the error detection. The unsuccessful slaves, if previously residing at a unique address, revert to the class address. The master receives the hardware identification (UID) of the successfully transmitting slave and issues a Set Address command in combination with the hardware identification (UID) and the new unique address to all slave agents at the class address. Only the slave agent with a hardware identification (UID) matching the UID of the Set Address command processes the Set Address command to completion and is assigned the address. The master uses the Get Bitwise UID command followed by the Set Address command in a loop to locate, identify and assign addresses to agents responding to a predetermined class address.

31 Claims, 6 Drawing Sheets



United States Patent [19]
Boudreau

[11] **Patent Number: 4,511,960**
[45] **Date of Patent: Apr. 16, 1985**

[54] **DATA PROCESSING SYSTEM AUTO ADDRESS DEVELOPMENT LOGIC FOR MULTIWORD FETCH**

[75] Inventor: Daniel A. Boudreau, Billerica, Mass.
[73] Assignee: Honeywell Information Systems Inc., Waltham, Mass.

[21] Appl. No.: 239,569
[22] Filed: Jan. 16, 1981
[51] Int. Cl.³ G06F 9/10; G06F 9/32; G06F 13/00
[52] U.S. Cl. 364/200; 364/931
[58] Field of Search ... 364/200 MS File, 900 MS File, 364/931; 307/440; 371/16, 17

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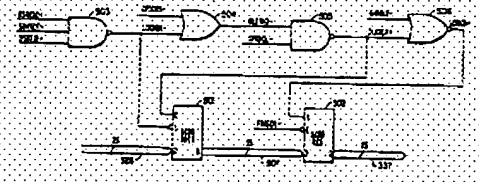
IBM Tech. Discl. Bull., vol. 16, No. 2, Jul. 1973; "Computer Performance Measurement", L. A. Belady et al., pp. 455-456.

Primary Examiner—Raulfe B. Zache
Assistant Examiner—William G. Niessen
Attorney, Agent, or Firm—William A. Linnell; Nicholas Prasinos

[57] **ABSTRACT**

An auto address development logic that, when provided a starting address, is used to develop consecutive addresses as multiple words of information are presented, one word at a time, during multiple consecutive information transfer cycles. The logic retains for use a current address while simultaneously developing the next address so that the next address will be immediately available as the current address at the beginning of the next information transfer cycle. The auto address development logic is used in a system analyzer connected to a data processing system having a common bus over which the CPU, during a first bus cycle, provides a starting address and requests that the memory fetch multiple words of information which are transferred to the CPU, during multiple subsequent responding bus cycles.

1 Claim, 17 Drawing Figures



Refine Search

Search Results -

Terms	Documents
L2 same bus same master same slave	11

Database:

- US Pre-Grant Publication Full-Text Database
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Search: L3

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Search History

DATE: Monday, August 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same bus same master same slave	11	L3
L2	(address$3 near3 auto$6)	5135	L2
L1	(address$3 near3 auto$6) same (multiplex$3 adj1 bus)	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2 same bus same master same slave	0

Database:

US Pre-Grant Publication Full-Text Database
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Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L2 same bus same master same slave	0	L4
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	L2 same bus same master same slave	11	L3
L2	(address$3 near3 auto$6)	5135	L2
L1	(address$3 near3 auto$6) same (multiplex$3 adj1 bus)	2	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/245 |370/254 |370/471 |370/457 |370/475 |379/21.14 |710/104 |710/110 |710/9 |710/62 |710/3 |700/24 |340/825.52 |340/3.5).ccls.	6769

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	710/104,110,9,62,3;370/254,471,457,475;340/825.52,3.5;379/21.14;700/24;709/245.ccls.	6769	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L2	52

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L3

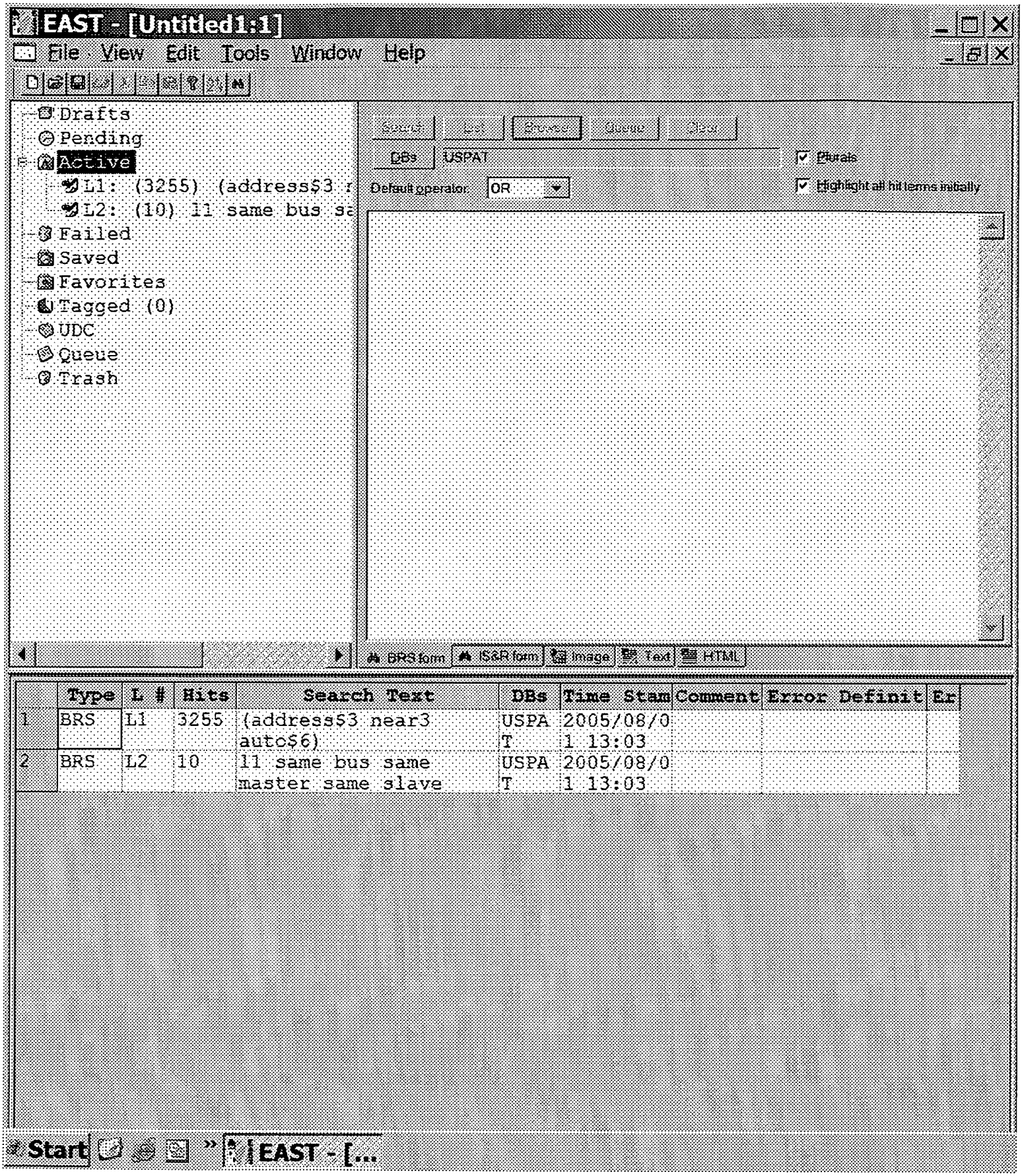
Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 01, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	l1 and L2	52	L3
L2	(address$3 near3 auto$6) same bus 221/14	460	L2
L1	710/104,110,9,62,3;370/254,471,457,475;340/825.52,3.5;379/21.14;700/24;709/245.ccls.	6769	L1

END OF SEARCH HISTORY


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (3255) (address$3 r
L2: (10) 11 same bus sa
Failed
Saved
Favorites
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Default operator:
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Highlight all hit terms initially
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IS&R form
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Search Text
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Er
1
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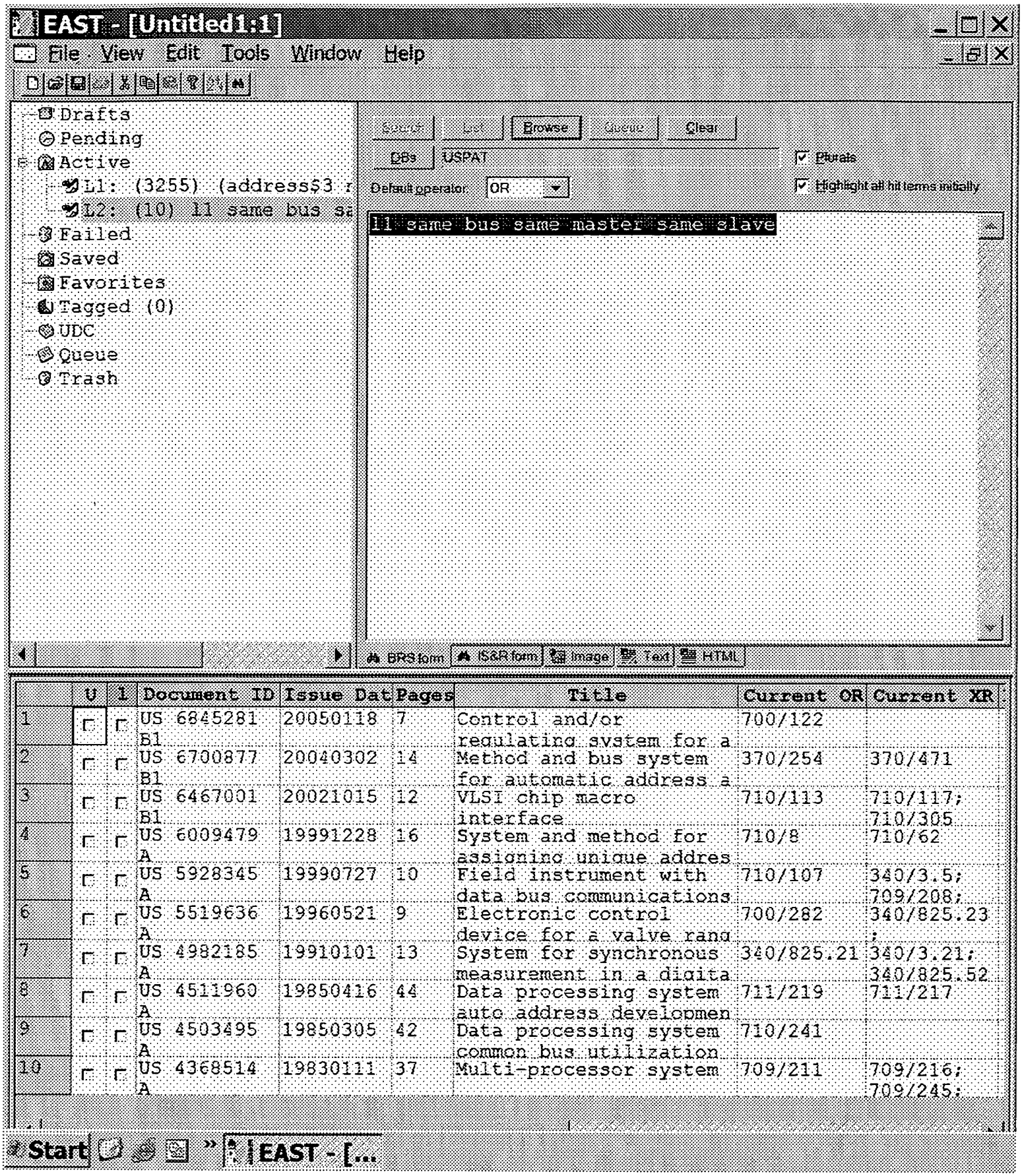
3255
(address$3 near3 auto$6)
USPA T
2005/08/0 1 13:03
2
BRS
L2
10
11 same bus same master same slave
USPA T
2005/08/0 1 13:03
Start
EAST - [...


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (3255) (address$3 r
L2: (10) l1 same bus sa
Failed
Saved
Favorites
Tagged (0)
UDC
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USPAT
Plurals
Default operator:
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l1 same bus same master same slave
BRS form
IS&R form
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HTML
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Document ID
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Pages
Title
Current OR
Current XR
1 US 6845281 B1 20050118 7 Control and/or regulating system for a 700/122
2 US 6700877 B1 20040302 14 Method and bus system for automatic address a 370/254 370/471
3 US 6467001 B1 20021015 12 VLSI chip macro interface 710/113 710/117; 710/305
4 US 6009479 A 19991228 16 System and method for assigning unique addres 710/8 710/62
5 US 5928345 A 19990727 10 Field instrument with data bus communications 710/107 340/3.5; 709/208;
6 US 5519636 A 19960521 9 Electronic control device for a valve rang 700/282 340/825.23 ;
7 US 4982185 A 19910101 13 System for synchronous measurement in a digita 340/825.21 340/3.21; 340/825.52
8 US 4511960 A 19850416 44 Data processing system auto address developmen 711/219 711/217
9 US 4503495 A 19850305 42 Data processing system common bus utilization 710/241
10 US 4368514 A 19830111 37 Multi-processor system 709/211 709/216; 709/245;
Start
EAST - [...

Results for "(auto<in>metadata) <and> (address*<in>metadata) and bus"

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(auto<in>metadata) <and> (address*<in>metadata) and bus

Check to search only within this results set

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Display Format: Citation Citation & Abstract

Select Article Information

1. **A complete compiler approach to auto-parallelizing C programs for multi-DSP systems**
Franke, B.; O'Boyle, M.F.P.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 16, Issue 3, Mar 2005 Page(s):234 - 245
Digital Object Identifier 10.1109/TPDS.2005.26
AbstractPlus | Full Text: PDF(1136 KB) IEEE JNL

2. **A multimicroprocessor system with distributed common memory for real-time digital correlation and spectrum analysis**
Ganesan, S.; Ahmad, M.; Swamy, M.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '85.
Volume 10, Apr 1985 Page(s):1609 - 1612
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3. **Computer-based design for tomorrow's super chip**
Solomon, J.;
Solid-State Circuits Conference. Digest of Technical Papers. 1986 IEEE International
Volume XXIX, Feb 1986 Page(s):54 - 55
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4. **Dynamic reconfiguration of telecom services architectures according to mobility and traffic models**
Letaifa, A.B.; Choukair, Z.; Tabbane, S.;
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5. **Combining program recovery, auto-parallelisation and locality analysis for C programs on multi-processor embedded systems**
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A complete compiler approach to auto-parallelizing C programs for multi-DSP systems

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This paper appears in: **Parallel and Distributed Systems, IEEE Transactions on**
Publication Date: Mar 2005
Volume: 16 , Issue: 3
On page(s): 234 - 245
ISSN: 1045-9219
INSPEC Accession Number:8321674
Digital Object Identifier: 10.1109/TPDS.2005.26
Posted online: 2005-01-31 08:28:21.0

Abstract

Auto-parallelizing compilers for embedded applications have been unsuccessful due to the widespread use of pointer arithmetic and the complex memory model of multiple-**address** space digital signal processors (DSPs). This work develops, for the first time, a complete **auto**-parallelization approach, which overcomes these issues. It first combines a pointer conversion technique with a new modulo elimination transformation for program recovery enabling later parallelization stages. Next, it integrates a novel data transformation technique that exposes the processor location of partitioned data. When this is combined with a new **address** resolution mechanism, it generates efficient programs that run on multiple **address** spaces without using message passing. Furthermore, as DSPs do not possess any data cache structure, an optimization is presented which transforms the program to both exploit remote data locality and local memory bandwidth. This parallelization approach is applied to the DSPstone and UTDSP benchmark suites, giving an average speedup of 3.78 on four analog devices TigerSHARC TS-101 processors.

Index Terms

Inspec

Controlled Indexing

C language digital signal processing chips embedded systems message passing multiprocessor interconnection networks parallel memories parallel processing parallelising compilers program compilers reverse engineering

Non-controlled Indexing

TigerSHARC TS-101 processors **address** resolution mechanism **auto**-parallelizing C program complete compiler approach complex memory model data transformation technique embedded application interprocessor communication local memory bandwidth message passing multiDSP system multiple **address** space digital signal processor parallel processors pointer conversion technique real-time application remote data locality reverse engineering

Author Keywords

Parallel processors and reengineering arrays compilers conversion from sequential to parallel forms evaluation interprocessor communications measurement modeling performance measures real-time and embedded systems restructuring reverse engineering signal processing systems simulation of multiple-processor systems

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L3: Entry 1 of 11 File: PGPB Jun 9, 2005

PGPUB-DOCUMENT-NUMBER: 20050125579
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050125579 A1

TITLE: Binary-coded, auto-addressing system and method

PUBLICATION-DATE: June 9, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Bui, Tanh M.	Cary	NC	US	
Stockfisch, Reiner E.	Furth		DE	
Taufer, Tobias	Roth		DE	

US-CL-CURRENT: 710/104; 710/110, 710/9

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6845281 B1

L3: Entry 2 of 11 File: USPT Jan 18, 2005

US-PAT-NO: 6845281
DOCUMENT-IDENTIFIER: US 6845281 B1

TITLE: Control and/or regulating system for a machine used for producing a fiber web

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6700877 B1

L3: Entry 3 of 11 File: USPT Mar 2, 2004

US-PAT-NO: 6700877
DOCUMENT-IDENTIFIER: US 6700877 B1

TITLE: Method and bus system for automatic address allocation

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 6467001 B1

L3: Entry 4 of 11 File: USPT Oct 15, 2002

US-PAT-NO: 6467001
DOCUMENT-IDENTIFIER: US 6467001 B1

TITLE: VLSI chip macro interface

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 5. Document ID: US 6009479 A

L3: Entry 5 of 11 File: USPT Dec 28, 1999

US-PAT-NO: 6009479
DOCUMENT-IDENTIFIER: US 6009479 A

TITLE: System and method for assigning unique addresses to agents on a system management bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 6. Document ID: US 5928345 A

L3: Entry 6 of 11 File: USPT Jul 27, 1999

US-PAT-NO: 5928345
DOCUMENT-IDENTIFIER: US 5928345 A

TITLE: Field instrument with data bus communications protocol

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 5519636 A

L3: Entry 7 of 11 File: USPT May 21, 1996

US-PAT-NO: 5519636
DOCUMENT-IDENTIFIER: US 5519636 A

TITLE: Electronic control device for a valve range of modular design

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 4982185 A

L3: Entry 8 of 11 File: USPT Jan 1, 1991

US-PAT-NO: 4982185
DOCUMENT-IDENTIFIER: US 4982185 A

TITLE: System for synchronous measurement in a digital computer network

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 9. Document ID: US 4511960 A

L3: Entry 9 of 11 File: USPT Apr 16, 1985

US-PAT-NO: 4511960
DOCUMENT-IDENTIFIER: US 4511960 A

TITLE: Data processing system auto address development logic for multiword fetch

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 10. Document ID: US 4503495 A

L3: Entry 10 of 11 File: USPT Mar 5, 1985

US-PAT-NO: 4503495
DOCUMENT-IDENTIFIER: US 4503495 A

TITLE: Data processing system common bus utilization detection logic

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Terms	Documents
L2 same bus same master same slave	11

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L3: Entry 1 of 11 File: PGPB Jun 9, 2005

PGPUB-DOCUMENT-NUMBER: 20050125579
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20050125579 A1

TITLE: Binary-coded, auto-addressing system and method

PUBLICATION-DATE: June 9, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Bui, Tanh M.	Cary	NC	US	
Stockfisch, Reiner E.	Furth		DE	
Taufer, Tobias	Roth		DE	

APPL-NO: 10/ 727053 [PALM]
DATE FILED: December 4, 2003

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 710/104; 710/110, 710/009
US-CL-CURRENT: 710/104; 710/110, 710/9

REPRESENTATIVE-FIGURES: 3

ABSTRACT:

A system and method for auto-addressing devices on a multiplexing bus in which a plurality of devices are arranged in series, with each having a bus in and bus out. During an initial evaluation, and beginning with a low bus in, each device inverts the incoming signal so that a device with a low bus in has a high bus out. During a second evaluation, the high or low state of the bus in is inverted only if the bus out in the first evaluation was high. Similarly, during a third (and subsequent) evaluation, the high or low state of the bus in is inverted only if the bus out state of all previous evaluations was high. Ultimately, only one device will have a high bus out, with all bus out states from previous evaluations also having been high, at which point all addresses are fully decoded. The system works equally well with a "low bus out" of all evaluations being used to determine inversion.

Previous Doc Next Doc Go to Doc#

L3: Entry 3 of 11 File: USPT Mar 2, 2004

US-PAT-NO: 6700877
DOCUMENT-IDENTIFIER: US 6700877 B1

TITLE: Method and bus system for automatic address allocation

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lorenz; Joachim	Hemhofen			DE
Weber; Karl	Altdorf			DE

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Siemens Aktiengesellschaft	Munich			DE	03

APPL-NO: 09/ 485212 [PALM]
DATE FILED: February 4, 2000

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	197 33 906	August 5, 1997

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102(E)-DATE
PCT/DE98/02076	July 23, 1998	WO99/08164	Feb 18, 1999		

INT-CL: [07] H04 L 12/28

US-CL-ISSUED: 370/254; 370/471
US-CL-CURRENT: 370/254; 370/471

FIELD-OF-SEARCH: 370/254, 370/471, 370/457, 340/825.52, 714/48

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5636342	June 1997	Jeffries	714/48
☐	5689675	November 1997	Buij et al.	340/825.52
☐	5768277	June 1998	Ohno et al.	
☐	5848072	December 1998	Prill et al.	370/471

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
37 36 081	May 1989	DE	
44 28 502	February 1996	DE	
0 173 905	March 1986	EP	
08 037538	February 1996	JP	
WO 99/49397	September 1999	WO	

ART-UNIT: 2661

PRIMARY-EXAMINER: Cangialosi; Salvatore

ATTY-AGENT-FIRM: Staas & Halsey LLP

ABSTRACT:

A method for automatic address assignment is disclosed, said method being based on a distance measurement, a master (M) transmitting via the bus a preamble (P) which is received by all the slaves which are to be addressed. The slaves react to the preamble (P) by transmitting a response signal sequence (A). A slave (S2) which is located upstream, in the direction of the master (M), of a slave (S3) which transmits a response signal sequence (A) registers the response signal sequence (A) of the slave (S3) and subsequently waits for a new preamble (P). The slave (Sz) which does not register any response signal sequences (A) from other slaves is the last slave (Sz), seen from the master (M), without address allocation on the bus. This slave (Sz) switches into a state in which it is ready to receive an address-assigning telegram (T) from the master (M), with which address-assigning telegram (T) it is assigned an unambiguous address. During the next cycle of the method, the slave (Sz) which has just been assigned an address no longer reacts to the preamble (P) so that another slave evaluates the constellations at the bus in such a way that it switches into a state in which it is ready to receive the address-assigning telegram. In this way, all the slaves without an address are gradually assigned an address.

17 Claims, 5 Drawing figures

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